CLAIMS

I Claim:

1. A method of accessing data in a data processing system having a graphics engine, the method comprising:

accessing a first portion of a frame of graphics data through a first channel of memory;

accessing a second portion of a frame of graphics data through a second channel of memory;

accessing system data through the first channel of memory simultaneously with the step of accessing the second portion of a frame of graphics data through the second channel of memory.

2. The method of claim 1, wherein the first portion and second portion are logically consecutive blocks of graphics data.

3. The method of claim 2, wherein the logically consecutive blocks are for storing horizontally adjacent pixel matrices.

4. The method of claim 2, wherein the logically consecutive blocks are for storing vertical adjacent pixel matrices.

5. The method of claim 1, wherein the first channel accesses data on first clock edge, and the second channel accesses data on a second clock edge, wherein the first clock edge and the second clock edge are skewed from one another.

6. The method of claim 1, wherein:

the step of accessing the first portion of a frame of graphics data through a first channel includes the first portion being a first type of graphics memory;

the step of accessing a second portion of a frame of graphics data through a second channel includes the second portion being a second type of graphics memory;

7. The method of claim 6, wherein the step of accessing the first portion and the step of accessing a second portion are performed substantially simultaneously.

8. The method of claim 6, wherein the first portion of a frame of graphics data and the second portion of a frame of graphics data are associated with a common pixel.

9. The method of claim 6, wherein the first type is z graphics data, and the second type is destination graphics data.

10. A method of partitioning memory in a data processing system, the method comprising:

identifying a first portion of a memory associated with a first channel as graphics memory;

identifying a second portion of a memory associated with a second channel as graphics memory;

partitioning each of the first and a second portion of memory into blocks;

mapping each of the blocks to an X-Y location, wherein each block associated with a first channel is horizontally and vertically adjacent to blocks associated with the second channel.

11. A method of accessing data in a data processing system, the method comprising the steps of:

storing a first data to one of a first memory and a second memory, wherein the first memory is associated with a first memory channel, the second memory is associated with a second memory channel, and the first data is associated with a first location of a video image and has a first video data type.

storing a second data to one of the first and second memory, wherein the second data is associated with the first location of the video image and has a second video data type, and is stored in a different memory than the first data.

12. The method of claim 11, wherein the first data type is a Z-data associated with a three-dimensional image.

13. The method of claim 12, wherein the second data type is a destination (DST) data associated with a three-dimensional image.

14. The method of claim 11, further comprising the steps of:

storing a third data to one of the first and second memory, wherein the third data is associated with a second location of a video image, has the first video data type, and is stored in a different memory that the first data.

storing a fourth data to one of the first and second memory, wherein the second data is associated with the second location of the video image, has the second video data type, and is stored in a different memory than the third data.

15. A method of partitioning data, the method comprising:

determining the memory present in a system;

partitioning the memory between a first channel and a second channel;

partitioning a first portion of the memory associated with the first channel as system memory;

partitioning a second portion of the memory associated with the first channel as graphics memory; and

partitioning at least a portion of the memory associated with the second channel as graphics memory.

16. The method of claim 15, wherein the graphics memory associated with the first channel and the graphics memory associated with the second channel are arranged in blocks of data having adjacent physical addresses.

17. The method of claim 16, wherein the adjacent physical addresses are arranged in rows and columns so that each block associated with a row and column is adjacent to a block accessed by a different channel.

18. A data processing system comprising:

a system controller having:

a first memory channel controller;

a second memory channel controller; and

a high-speed PCI bus arbiter;

an input output (IO) controller coupled to the high-speed PCI bus arbiter, and having a low-speed PCI bus arbiter, wherein the low speed PCI arbiter supports a slower PCI bus rate than the high-speed PCI bus arbiter.

19. The system of claim 18, wherein a bus rate of the high speed PCI bus arbiter is at least 10 percent faster than the bus rate of the low speed PCI bus arbiter.

20. The system of claim 19, wherein the bus rate of the high speed PCI bus arbiter is approximately 66 Mbits per second per data pin and the bus rate of the low speed PCI bus arbiter is approximately 33 Mbits per second per data pin.

21. The system of claim 18, further comprising a data storage device coupled to the IO device to transmit data at a data rate higher that the data rate of the low-speed PCI bus arbiter.

22. A system comprising:

a first controller having an arbiter to arbitrate requests for a first bus of a predefined protocol type at a first data rate; and

an second controller having:

an arbiter to arbitrate requests for a second bus of the predefined protocol type at a second data rate, wherein the first data rate is at least 10 percent greater than the second data rate; and

control circuitry to interface to the first bus.

23. The system of claim 22, further comprising:

an IO device coupled to the control circuitry of the second controller without being coupled to the arbiter of the IO controller.